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Noise Analysis of Current-Mode Preamplifier Circuit

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ABSTRACT
Noise is an inherent property of any electrical circuit such as shot noise due to P-N junction, thermal noise due to thermal excitation of charge carriers etc. The limit to sensitivity of an electrical circuit is set by the point at which the signal to noise ratio drops below acceptable limits. The existence of noise in CMOS circuits is due to the fact that electrical charge is not continuous but is carried in discrete amounts equal to the charge of an electron. The most important component of a bio-signal acquisition system is the front end amplifier and a preamplifier circuit is an important stage of that acquisition system. In this paper, we analyze a preamplifier circuit for certain dominant noise to minimize the same.

Keywords **-** Aspect ratio, Current-mode preamplifier, Flicker Noise, Noise Spectral density, Signal to Noise ratio, Thermal Noise.

I. INTRODUCTION

In many cases noise found on a signal in a circuit is unwanted. When creating a circuit one usually wants a true output of what the circuit has accomplished. A low-noise wideband current preamplifier is the fundamental input stage in those on-chip systems devoted to high resolution measuring applications. For these applications the preamplifier should feature a very low capacitance at the input node to limit high frequency noise. Also a large dynamic range is required for the preamplifier circuit. We can express dynamic range as Signal to Noise ratio (SNR). If the preamplifier is nonlinear, then a pure sinusoidal signal will generate harmonics. When the Total Harmonic Distortion (THD) of these exceeds noise, then nonlinearity becomes the limiting factor. The notation of Signal to Noise Ratio plus Distortion (SNRD) can be used to define both noise and distortion in dynamic range considerations. The influence of signals such as charge injection and power supply injection is not considered and the Current mode preamplifier is considered to be linear, only the noise is considered.

This paper presents the analysis of the noise present in current mode preamplifier circuit. Section II describes the noise model of a single MOSFET which presents the background for noise analysis of current mode preamplifier circuit which is discussed in Section III..

II. BACKGROUND

The A low noise wideband current mode preamplifier is the fundamental input stage in on-chip systems devoted to high resolution measuring applications. The presence of noise in the amplifier circuit means that there is a lower limit below which signals cannot be amplified without significant distortion. Electrical noise can be modeled as a current source in parallel with the drain current of a MOSFET. This current source represents thermal and flicker (1/f) noise. The mean square current noise (iN2) defines the current source and is given by (1)

$$\overline{i_N^2} = \left[\frac{8kTg_m(1+\eta)}{3} + \frac{(KF)I_D}{fC_{ox}L^2}\right]\Delta f \qquad (A^2) \qquad (1)$$

The mean square voltage noise e_n^2 form can be obtained by dividing (1) by g_m^2

$$\overline{e_n^2} = \left[\frac{8kT(1+\eta)}{3g_m} + \frac{KF}{2fC_{ox}WLK'}\right]\Delta f \qquad (V^2) \qquad (2)$$

Where Δf is a small bandwidth at a frequency f, $\eta = g_{mbs}/g_m$, k is Boltzmann's constant, T is temperature (K), gm is small signal trans-conductance from gate to channel, KF is flicker noise coefficient(F-A). The equivalent input-mean-square voltage-noise from (2) will be useful for analyzing the noise performance of preamplifier circuit in section III.

And from various experimental results 1/f noise and thermal noise are the dominant in CMOS circuits for frequencies below 100 KHz compared to shot noise, burst noise and avalanche noise. The shot noise is mostly a concern in bipolar transistor [2] and is negligible in CMOS technology. Another significant noise source is thermal which occurs in both the resistors and channel of MOSFETs. For MOS transistors, thermal noise is typically represented by thermal noise drain current $\overline{I_n^2}$. For transistors of trans-conductance gm

$$\overline{I_n^2} = 4kT\gamma g_m \qquad (3)$$

where γ is the thermal noise coefficient which is 2/3 for long channel transistors and larger for deep sub micron MOSFET.

Other kinds of thermal noise such as resistive gate thermal noise, are usually negligible as compared with previous noise source and therefore can be neglected in noise calculation. If the bias current is reduced, the thermal noise floor increases, thus moving the 1/f noise corner to a lower frequency. Therefore, the 1/f noise corner is a function of the thermal noise floor. Consequently, in many practical cases, the equivalent input-mean-square voltage noise of equation (2) is simplified to equation (4) taking into consideration of thermal noise term only (second term in equation 2).

$$\overline{e_{eq}^2} = \left[\frac{KF}{2fC_{ox}WLK'}\right]\Delta f \quad (V^2) \qquad (4)$$

In terms of the input-voltage noise spectral density equation (4) can be re-written as noise performance.

$$\overline{e_{eq}^2} = \frac{e_{eq}^2}{\Delta f} = \frac{KF}{2fC_{ox}WLK'} = \frac{B}{fWL}(V^2/Hz) \qquad (5)$$

where B is a constant for an n-channel or a p-channel device of a given process. The RHS of equation (5) is important in optimizing the design with respect to noise performance.

III. NOISE ANALYSIS OF PREAMPLIFIER CIRCUIT

The The most important component of a bio-signal acquisition system is the front end amplifier. The Front-End Amplifier (FEA) is one of the key elements in the acquisition device, which senses and amplifies the neural signals such as Electrocorticography (ECoG), Electrocardiogram (ECG), action potential, local field potential (LFP) etc., through electrode-tissue interfaces. Since the amplitude of neural signals is very small and the electrodes are easily interfered by external noise sources like 60-Hz noise from power lines or other disturbance sources, a low-noise FEA is required.
Figure 2 shows a CMOS preamplifier that achieves low noise by careful selection of the W/L ratios. The compensation capacitor to the source of M11 allows the output pole to be increased. PMOS devices are selected for the preamplifier ignoring the noise contributed by the dc current sources. The current sources can be ignored because their gates are usually connected to low impedance.

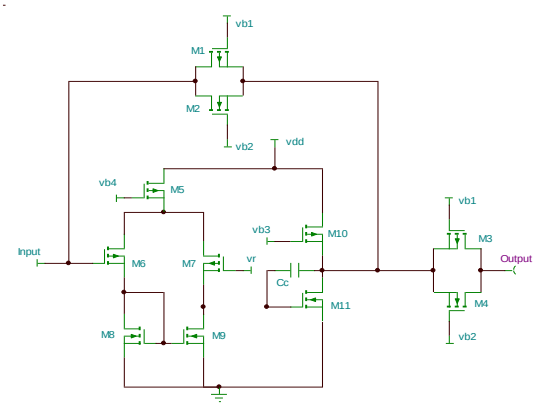

Figure1. CMOS current mode preamplifier circuit

The first approach for minimizing the 1/f noise uses circuit topology and transistor selection. Empirically, NMOS transistors have about two to five times more 1/f noise than PMOS transistors. Therefore, PMOS transistors should be used where it is important to reduce the 1/f noise. The one principle that is key in minimizing noise is to make the first stage gain as high as possible. This means that if the input is a differential amplifier, the source coupled transistors should be PMOS and the gain of the differential amplifier must be as large as possible. And the lengths of the load transistors should be greater than the lengths of the input transistors to minimize the 1/f noise.

The noise model of Fig.1 is shown in Fig.2. The noise contributed by M5 in this model is ignored because it acts as a current source.

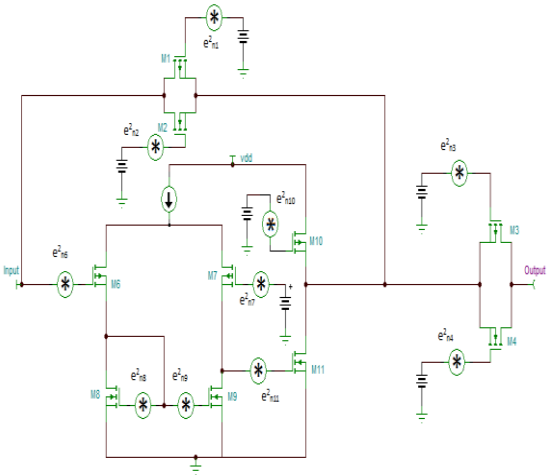

Figure 2.The noise model for circuit diagram in figure 1.

The input referred current noise In of the current mode preamplifier can be expressed as

$$\overline{(I_n^2)} = \left[\frac{kT}{3}\left(g_{m_{Mn\,1}} + g_{m_{Mp\,1}}\right) + (2\pi f)^2 c_{in}^2 \overline{\left(e_{eq}^2\right)}\right]\Delta f \qquad (6)$$

where k is Boltzmann constant, T is the absolute temperature, gm is the trans-conductance of MOS

device, f is the signal frequency, Cin is the input capacitance of OP1, and Δf is the bandwidth of the preamplifier[3].

The first term in (6) is mainly contributed by M1/M2 and we observe, I2n is proportional to trans-conductance gm of MOS devices. Hence, for low noise per performance the devices M1/M2 should have low dc currents. Therefore M3/M4 are operated at low dc currents and the noise contribution to the equivalent input noise is divided by the gain α offered by the M1(M2) and M3(M4) combination. (Since they are operated at low dc current in the linear sub-threshold region as resistors and channel lengths of M1(M2) and M3(M4) are kept same, the resistance ratio of M1(M2) to M3(M4) is equal to channel width ratio of M1(M2) to M3(M4) say α. With small signal input current i1 flowing on M1(M2) the small signal voltage across M1(M2) is same as that of M3(M4). Thus the current i2 on M3(M4) is equal to α times i1 and hence a current gain of α can be achieved).

The second term in equation (6) is contributed by the flicker noise en,eq_flicker and the thermal noise en,eq_thermal of the op-amp stage.

$$e_{eq}^2 = e_{eq_{thermal}}^2 + e_{eq_{flicker}}^2 \quad (7)$$

$$\overline{(e_{to}^2)} = g_{m11}R_0^2[e_{n11}^2 + e_{n10}^2 + R_i^2(g_{m6}^2 e_{n6}^2 + gm72en72 + gm82en82 + gm92en92 \quad (8)$$

Where e2to is total output-voltage-noise spectral density, Ro is the output resistance seen at the drain of M11 and Ri is the input resistance seen at the gate of M1.

The equivalent input-voltage-noise spectral density can be found by dividing (8) by the differential gain of op-amp (gm6Rigm11Ro)2to get

$$e_{eq}^2 = \frac{e_{to}^2}{(g_{m6}g_{m11}R_iR_o)^2}$$

$$= \frac{2e_{n11}^2}{g_{m6}^2R_i^2} + 2e_{n6}^2\left[1 + \left(\frac{g_{m8}}{g_{m6}}\right)^2\left(\frac{e_{n8}^2}{e_{n6}^2}\right)^2\right] \quad (9)$$

with e2n11=e2n10, e2n8=e2n9 and e2n6=e2n7. From equation (9) it is observed that the second stage is divided by the gain of the first stage and therefore can be neglected. Hence the resulting equivalent input voltage noise spectral density can be approximately represented as

$$e_{eq}^2 = 2e_{n6}^2\left[1 + \left(\frac{g_{m8}}{g_{m6}}\right)^2\left(\frac{e_{n8}^2}{e_{n6}^2}\right)\right] \quad (10)$$

The model to be equated to the spectral density noise sources in Fig 2 is (because focusing on 1/f noise)

If the source is voltage,

$$e_{ni}^2 = \frac{B}{fW_iL_i}\left(V^2/Hz\right) \quad (11)$$

If the source is current,

$$i_{ni}^2 = \frac{2BK'I_i}{fL_i^2}\left(A^2/Hz\right) \quad (12)$$

Substituting equation (12) in equation (10)

$$e_{eq}^2 = 2e_{n6}^2\left[1 + \left(\frac{K_N'B_N}{K_p'B_P}\right)\left(\frac{L_6}{L_8}\right)^2\right]\left(V^2/Hz\right) \quad (13)$$

Hence to minimize the noise, the above equation for e2eq must be minimized. And since PMOS devices are selected as input (M6 and M7) the value of e2n6 is minimized if product of W6 and L6 (W7 and L7) is large. And to minimize it further it is necessary to choose the ratio of L6 and L7 properly which can be less than 1(it gives an equivalent input noise spectral density of 2e2n6).

Also the flicker noise for the op-amp in the preamplifier circuit can be approximately expressed as

$$e_{eq\ flicker}^2 = \frac{2}{C_{ox}f}\left[\frac{K_p}{W_6L_6} + \frac{\mu_nK_nL_6}{\mu_pW_6L_8^2}\right] \quad (14)$$

Therefore the flicker noise is inversely proportional to L28 and so M8 should be designed with long device channel length to reduce the flicker noise. To avoid the effect of long length in limiting the signal swings M8 should be designed with large device width W8, since the input noise is independent of W8 large W8 does not increase the noise. W6 is also designed to be larger to reduce both thermal and flicker noises.

And thermal noise can be approximated as

$$e_{eq_{thermal}}^2 \approx \frac{16kT}{3}\frac{1}{g_m^2[g_{m6}+g_{m7}]} \quad (15)$$

Hence thermal noise can be reduced by increasing gm1. Thus, the bias current is increased to increase gm1 and reduce the thermal noise contributed to the preamplifier.

IV. CONCLUSION

Flicker noise and thermal noise are dominant in CMOS circuits. These can be minimized by carefully selecting the channel length and width for MOSFETs. Also selecting PMOS devices for input reduces flicker noises. And the product of W and L should be large as possible with channel length being a large value for MOS devices. The above design equations are also applicable to various other CMOS circuits in cases where noise reduction is of great importance.

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